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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,368	08/13/2001	Hisaya Mori	50090-332	4507

7590 03/14/2003

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EXAMINER
CHAN, EMILY Y

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,368	MORI ET AL.	
	Examiner	Art Unit	
	emily y chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amended claims 1-5 remain for examination, claim 6 has been cancelled and new claims 7-12 have been added.

Claims 8, 10 and 12 are objected to because of the following informalities:

In claims 8, the recitation "**digital test data derived from the digital-to-analog converter circuit in a second mode of operation**" and in claim 10 the recitation "**digital test data stored in the test ancillary device memory is derived from the digital-to-analog converter circuit converting the source digital signal to analog form**" are unclear. How the output of the D/A converter is in digital form is unclear. The output of the digital-to-analog converter circuit should be an analog data and not a digital data form.

In claim12, the recitation "**the test ancillary device does not store digital test data in the first digital test data**" is unclear. The examiner assumes that "the test ancillary device does not store digital test data in the first memory section". Appropriate correction is required.

The indicated allowability of claims 1-5 is withdrawn in view of the newly discovered reference(s) to Toshishige (01-316024) in view of Rosenthal et al ('521). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 -5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige (01-316024) in view of Yamamura ('019) and Rosenthal et al ('521).

With respect claim 1, Toshishige (01-316024) expressly teach an apparatus (see fig 1) for testing a semiconductor integrated circuit as claimed, comprising:

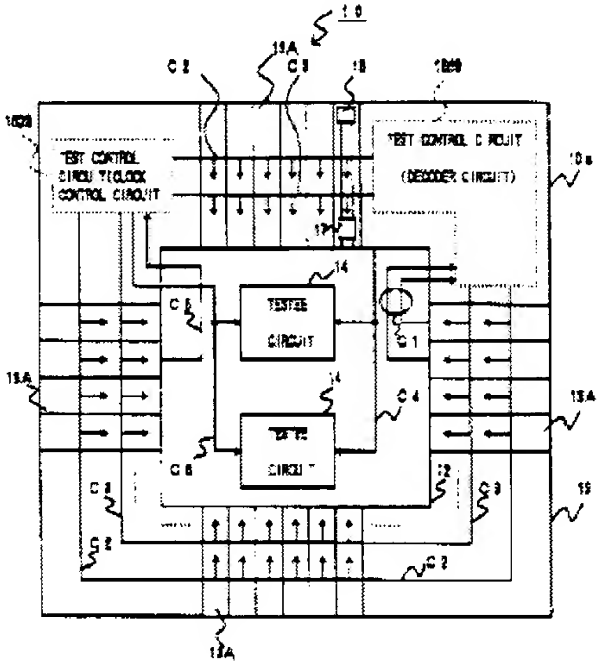
A ~~tester~~ (1) constructed so as to exchange a signal with a semiconductor integrated circuit (2) under test, the semiconductor integrated circuit (2) including an analog-to-digital converter circuit or a digital-to-analog converter circuit (3);

A test ancillary device (8, 6, 9, 11, 13 and 10) including data memory (11) for storing digital test data output from the analog-to-digital converter circuit (3) or digital test data produced by converting analog test data output from the digital-to-analog converter circuit (6), and an analysis section (10) for analyzing the digital data stored in the data memory (12).

Toshishige (01-316024) does not specify that his tester (1) and test ancillary device (8, 6, 9, 11, 13 and 10) are on a test board and his test ancillary device (8, 6, 9, 11, 13 and 10) is disposed in the vicinity of the test board.

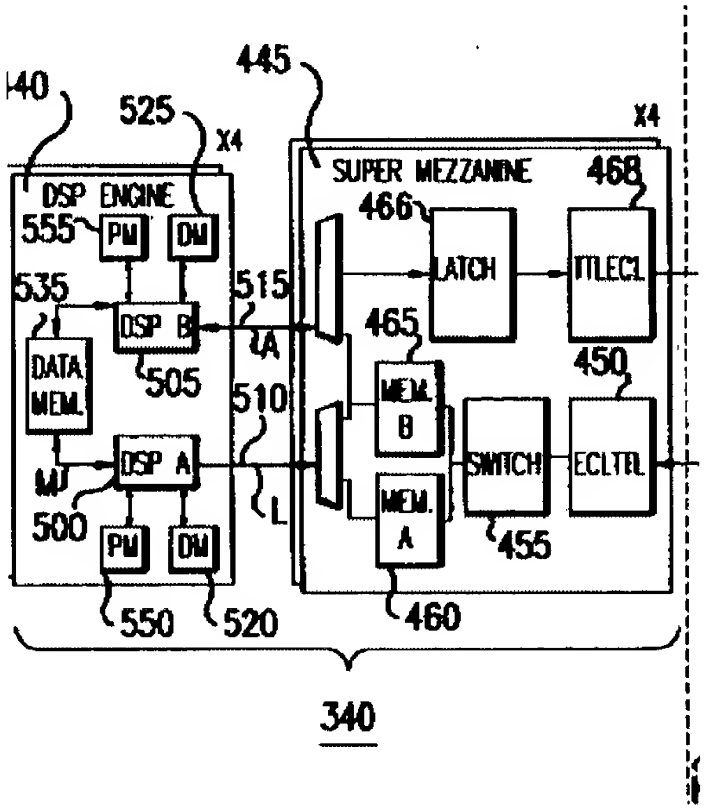
Yamamura ('019) discloses a semiconductor integrated circuit including a board (chip 10a) for testing functions of an internal circuit in a integrated circuit (see col. 1, lines 9-10) and specifically teach to have test ancillary device (15) disposed in the vicinity of the chip (see Fig 4, below)

FIG. 4



Toshishige (01-316024) also does not teach that his data memory (11) is divided into two memory sections such that, when digital test data is stored in one memory section, digital test data previously stored in the other memory section is loaded for analysis purpose.

Rosenthal et al ('521) disclose mixed-signal tester architecture of the IXD7232 board (fig 4, below and col. 7, lines 14-15) comprising multi-bank capture memory for storing test data and particularly teach when digital test data is stored in one memory section (460), digital test data previously stored in the other memory section (465) is loaded for analysis purpose (see Abstract, last 6 lines, and col. 7, lines 33-39).



It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Yamamura ('019) 's chip or board into Toshishige (01-316024)' apparatus for having easy connection between the test ancillary device and tester circuit as disclosed by Yamamura ('019) (see col. 6, lines 17-18). It also would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of the Rosenthal et al ('521)' test data multi-bank storing or capturing memory into Toshishige (01-316024)' apparatus for the purpose of speeding the test process as disclosed by Toshishige (01-316024)' (see abstract, last 2 lines).

With respect to claims 2 and 5, Rosenthal et al ('521)' teach first and second memory devices (460 and 465) which respectively include the first and second memory sections (multi-banks).

With respect to claims 3-4, Rosenthal et al ('521)' teach memory input and output changeover means (455) for performing a changeover operation on the test ancillary device memory (460, 465).

Claims 7, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige (01-316024) in view of Rosenthal et al ('521).

With respect claim 7, Toshishige (01-316024) expressly teach a method for testing a semiconductor integrated circuit (2) including at least one of an analog-to-digital converter circuit and a digital-to-analog converter circuit (3), a tester (1) configured to exchange one or more signals with the semiconductor integrated circuit (2) and a test ancillary device (8, 6, 9, 11, 13 and 10) coupled to the tester (1) including a memory (11) as claimed, comprising:

Storing first digital test data derived from the semiconductor integrated circuit (2) in the data memory (11) while providing second digital test data derived from the semiconductor integrated circuit (2) to an analysis device (10) configured to analyze digital test data stored in the data memory (11), wherein the first and second digital test data digital test data are one of output from the analog-to-digital converter circuit (6) or digital test data produced by converting analog test data output from the digital-to-analog converter circuit.

Toshishige (01-316024) does not teach that his data memory (11) is divided into two memory sections and the step that while providing second digital

test data derived from the semiconductor integrated circuit (2) and data previously stored in second memory section is loaded for analysis purpose.

Rosenthal et al ('521) disclose mixed-signal tester architecture of the IXD7232 board (fig 4, below and col. 7, lines 14-15) comprising multi-bank capture memory for storing test data and particularly teach when digital test data is stored in one memory section (460), digital test data previously stored in the other memory section (465) is loaded for analysis purpose (see Abstract, last 6 lines, and col. 7, lines 33-39).

It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Rosenthal et al ('521)' that allows data to be written into one band while previously-written data in another bank is processed into Toshishige (01-316024)' method for the purpose of speeding the test process as disclosed by Toshishige (01-316024)' (see abstract, last 2 lines).

With respect to claim 10, Toshishige (01-316024)' teach to provide a source digital signal (7) to the semiconductor integrated circuit (2), wherein the test data stored in the test ancillary device memory (11) is derived from the digital-to-analog converter circuit (3) converting the source digital signal (7) to analog form.

With respect to claims 11-12, Rosenthal et al ('521)' teach memory input and output changeover means (455) for performing a changeover operation on the test ancillary device memory (460, 465).

Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toshishige (01-316024) in view of Rosenthal et al ('521) as applied to claim 7 above, and further in view of Coggins et al ('365).

Toshishige (01-316024) in view Rosenthal et al ('521) do not teach to provide a source analog signal to semiconductor integrated circuit (2).

Coggins et al ('365) disclose a diagnostic apparatus for testing an analog circuit (see Fig 2) below and specifically teach that his semiconductor integrated circuit (15) includes both an analog-to-digital converter circuit (22) and digital –to-analog converter circuit (27), a source analog signal (see col.3, line 25) to the semiconductor integrated circuit (15).

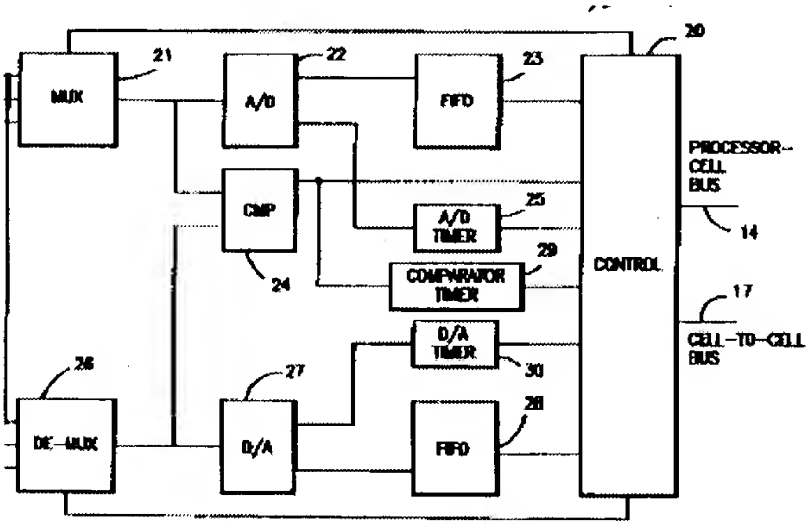


FIG. 2

It would have been obvious to one ordinary skill in the art at the time the invention was made to incorporate the teaching of Coggins et al's ('365) analog-to-digital converter circuit and digital-to-analog converter circuit into Tooshishige

(01-316024)' apparatus for the purpose of proviflexibility to perform various complex tests as disclosed by Coggins et al ('365) (see col. 2, lins 45-46).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y chan whose telephone number is 7033056123. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo, Kammie can be reached on 7033081233. The fax phone numbers for the organization where this application or proceeding is assigned are 7033085841 for regular communications and 7033085841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7022056123.

ec
March 7, 2003

KAMMIE CUNEO
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